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result set

*DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ*L8 L6 and l20 L8L7 L6 and l45 L7L6 graphic\$3 near2 (core or engine or block or module or unit or section
or accelerator or circuit\$3) near7 (super sampl\$3 or supersampl\$3)20 L6L5 l2 and l40 L5L4 graphic\$3 near2 (core or engine or block or module or unit or section
or accelerator or circuit\$3) near7 supersampl\$35 L4L3 graphic\$3 adj2 (core or engine or block or module or unit or section
or accelerator or circuit\$3) adj7 supersampl\$30 L3L2 (cpu or central proces\$4 or \$processor) adj3 (non-graphic\$3 or
nongraphic\$3)6 L2*DB=USPT; PLUR=YES; OP=ADJ*L1 (cpu or central proces\$4 or \$processor) adj3 (non-graphic\$3 or
nongraphic\$3)4 L1

END OF SEARCH HISTORY

WEST[Generate Collection](#)[Print](#)**Search Results - Record(s) 1 through 20 of 20 returned.**☐ 1. Document ID: US 20030076331 A1

L6: Entry 1 of 20

File: PGPB

Apr 24, 2003

DOCUMENT-IDENTIFIER: US 20030076331 A1

TITLE: Relative coordinates for triangle rendering

Detail Description Paragraph (16):

[0054] As shown in FIG. 3A, graphics board GB may comprise a graphics processing unit (GPU) 90, a super-sampled sample buffer 162, and one or more sample-to-pixel calculation units 170-1 through 170-V. Graphics board GB may also comprise one or more digital-to-analog converters (DACs) 178A-B.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	FIG	Draw Desc	Image
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☐ 2. Document ID: US 20030063095 A1

L6: Entry 2 of 20

File: PGPB

Apr 3, 2003

DOCUMENT-IDENTIFIER: US 20030063095 A1

TITLE: Statistic logic for collecting a histogram of pixel exponent values

Summary of Invention Paragraph (5):

[0005] A graphics accelerator may receive a stream a graphics data, and perform rendering computations to determine a stream of video pixels which are presented to a display device. The graphics accelerator may perform super-sampling and super-sample filtering to determine the video pixels. However, when using filters with negative lobes such as the truncated sync filter, it is possible to obtain negative pixel values even though all the super-sample values are non-negative quantities. Negative pixel values may need to be clamped to zero. The clamping to zero compromises visual quality of the output video. Thus, there exist a need for a system and methodology for controlling or minimizing the occurrence of negative pixels.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	FIG	Draw Desc	Image
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☐ 3. Document ID: US 20030011609 A1

L6: Entry 3 of 20

File: PGPB

Jan 16, 2003

DOCUMENT-IDENTIFIER: US 20030011609 A1

TITLE: Graphics system with real-time convolved pixel readback

Detail Description Paragraph (18):

[0067] FIG. 3 presents a block diagram for one embodiment of generic graphics board GB(K) for K=0, 1, 2, . . . , R-1. Graphics board GB(K) may comprise a graphics processing unit (GPU) 90, a super-sampled sample buffer 162, and one or more sample-to-pixel calculation units CU(0) through CU(V-1). Graphics board GB(K) may also comprise two digital-to-analog converters (DACs) 178A and 178B.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	EMMC	Draw Desc	Image
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☐ 4. Document ID: US 20020171653 A1

L6: Entry 4 of 20

File: PGPB

Nov 21, 2002

DOCUMENT-IDENTIFIER: US 20020171653 A1

TITLE: Splitting grouped writes to different memory blocks

CLAIMS:

3. The graphics system of claim 1, wherein the tile of graphics data comprises a number of elements, wherein the number of elements is greater than one, wherein each element is an independent unit of graphics data, wherein each independent unit of graphics data is a supersample, and wherein each supersample is a submultiple of a pixel.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	EMMC	Draw Desc	Image
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☐ 5. Document ID: US 20020158856 A1

L6: Entry 5 of 20

File: PGPB

Oct 31, 2002

DOCUMENT-IDENTIFIER: US 20020158856 A1

TITLE: Multi-stage sample position filtering

Detail Description Paragraph (16):

[0058] As shown in FIG. 3A, graphics board GB may comprise a graphics processing unit (GPU) 90, a super-sampled sample buffer 162, and one or more sample-to-pixel calculation units 170-1 through 170-V. Graphics board GB may also comprise one or more digital-to-analog converters (DACs) 178A-B.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	EMMC	Draw Desc	Image
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☐ 6. Document ID: US 20020122044 A1

L6: Entry 6 of 20

File: PGPB

Sep 5, 2002

DOCUMENT-IDENTIFIER: US 20020122044 A1

TITLE: Multi-spectral color correction

Detail Description Paragraph (18):

[0076] FIG. 3 presents a block diagram for one embodiment of generic graphics board

GB(K) for K=0, 1, 2, . . . , R-1. Graphics board GB(K) may comprise a graphics processing unit (GPU) 90, a super-sampled sample buffer 162, and one or more sample-to-pixel calculation units CU(0) through CU(V-1). Graphics board GB(K) may also comprise two digital-to-analog converters (DACs) 178A and 178B. In an alternative embodiment, graphics board GB(K) may include resources for operating on more than two simultaneous video channels, and thus, more than two digital-to-analog converters. In a second alternative embodiment, graphics board GB(K) may be configured to operate on a single video channel, and thus, may include only one digital-to-analog converter.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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KWIC	Draw Desc	Image
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☐ 7. Document ID: US 20020070944 A1

L6: Entry 7 of 20

File: PGPB

Jun 13, 2002

DOCUMENT-IDENTIFIER: US 20020070944 A1

TITLE: Graphics system having a super-sampled sample buffer with hot spot correction

Detail Description Paragraph (27):

[0164] FIG. 9 presents a block diagram for one embodiment of graphics board 116 according to the present invention. The following description of graphics board 116 generically describes any of graphics boards 113, 114 and 115. Graphics board 116 may comprise a graphics processing unit (GPU) 90, one or more super-sampled sample buffers 162, and one or more sample-to-pixel calculation units 170-1 through 170-V. Graphics board 116 may also comprise two digital-to-analog converters (DACs) 178A and 178B. In other embodiments, graphics board 116 may comprise more than two digital-to-analog converters.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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KWIC	Draw Desc	Image
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☐ 8. Document ID: US 20020050979 A1

L6: Entry 8 of 20

File: PGPB

May 2, 2002

DOCUMENT-IDENTIFIER: US 20020050979 A1

TITLE: Interpolating sample values from known triangle vertex values

Detail Description Paragraph (16):

[0066] As shown in FIG. 3A, graphics board GB may comprise a graphics processing unit (GPU) 90, a super-sampled sample buffer 162, and one or more sample-to-pixel calculation units 170-1 through 170-V. Graphics board GB may also comprise one or more digital-to-analog converters (DACs) 178A-B.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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KWIC	Draw Desc	Image
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☐ 9. Document ID: US 20020033828 A1

L6: Entry 9 of 20

File: PGPB

Mar 21, 2002

DOCUMENT-IDENTIFIER: US 20020033828 A1

TITLE: Flexible video architecture for generating video streams

Detail Description Paragraph (17):

[0081] FIG. 3 presents a block diagram for one embodiment of generic graphics board GB(K) for K=0, 1, 2, . . . , R-1. Graphics board GB(K) may comprise a graphics processing unit (GPU) 90, a super-sampled sample buffer 162, and one or more sample-to-pixel calculation units CU(0) through CU(V-1). Graphics board GB(K) may also comprise two digital-to-analog converters (DACs) 178A and 178B.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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KMCD	Draw Desc	Image
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☐ 10. Document ID: US 20020015052 A1

L6: Entry 10 of 20

File: PGPB

Feb 7, 2002

DOCUMENT-IDENTIFIER: US 20020015052 A1

TITLE: Graphics system configured to perform distortion correction

Detail Description Paragraph (28):

[0164] FIG. 9 presents a block diagram for one embodiment of graphics board 116 according to the present invention. The following description of graphics board 116 generically describes any of graphics boards 113, 114 and 115. Graphics board 116 may comprise a graphics processing unit (GPU) 90, one or more super-sampled sample buffers 162, and one or more sample-to-pixel calculation units 170-1 through 170-V. Graphics board 116 may also comprise two digital-to-analog converters (DACs) 178A and 178B. In other embodiments, graphics board 116 may comprise more than two digital-to-analog converters.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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KMCD	Draw Desc	Image
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☐ 11. Document ID: US 20020012004 A1

L6: Entry 11 of 20

File: PGPB

Jan 31, 2002

DOCUMENT-IDENTIFIER: US 20020012004 A1

TITLE: Blending the edges of multiple overlapping screen images

Detail Description Paragraph (27):

[0167] FIG. 9 presents a block diagram for one embodiment of graphics board 116 according to the present invention. The following description of graphics board 116 generically describes any of graphics boards 113, 114 and 115. Graphics board 116 may comprise a graphics processing unit (GPU) 90, one or more super-sampled sample buffers 162, and one or more sample-to-pixel calculation units 170-1 through 170-V. Graphics board 116 may also comprise two digital-to-analog converters (DACs) 178A and 178B. In other embodiments, graphics board 116 may comprise more than two digital-to-analog converters.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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KMCD	Draw Desc	Image
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☐ 12. Document ID: US 20020008697 A1

L6: Entry 12 of 20

File: PGPB

Jan 24, 2002

DOCUMENT-IDENTIFIER: US 20020008697 A1

TITLE: Matching the edges of multiple overlapping screen images

Detail Description Paragraph (27):

[0163] FIG. 9 presents a block diagram for one embodiment of graphics board 116 according to the present invention. The following description of graphics board 116 generically describes any of graphics boards 113, 114 and 115. Graphics board 116 may comprise a graphics processing unit (GPU) 90, one or more super-sampled sample buffers 162, and one or more sample-to-pixel calculation units 170-1 through 170-V. Graphics board 116 may also comprise two digital-to-analog converters (DACs) 178 A and 178 B. In other embodiments, graphics board 116 may comprise more than two digital-to-analog converters.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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KWIC	Draw Desc	Image
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☐ 13. Document ID: US 20020005854 A1

L6: Entry 13 of 20

File: PGPB

Jan 17, 2002

DOCUMENT-IDENTIFIER: US 20020005854 A1

TITLE: Recovering added precision from L-bit samples by dithering the samples prior to an averaging computation

Detail Description Paragraph (22):

[0078] FIG. 3 presents a block diagram for one embodiment of graphics board GB(I). Graphics board GB(I) may comprise a graphics processing unit (GPU) 90, one or more super-sampled sample buffers 162, and one or more sample-to-pixel calculation units 170-1 through 170-V. Graphics board GB(I) may also comprise two digital-to-analog converters (DACs) 178A and 178B. In other embodiments, graphics board GB(I) may comprise more or less than two digital-to-analog converters.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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KWIC	Draw Desc	Image
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☐ 14. Document ID: US 20020000988 A1

L6: Entry 14 of 20

File: PGPB

Jan 3, 2002

DOCUMENT-IDENTIFIER: US 20020000988 A1

TITLE: Rendering lines with sample weighting

Detail Description Paragraph (16):

[0077] As shown in FIG. 3A, graphics board GB may comprise a graphics processing unit (GPU) 90, a super-sampled sample buffer 162, and one or more sample-to-pixel calculation units 170-1 through 170-V. Graphics board GB may also comprise one or more digital-to-analog converters (DACs) 178A-B.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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KWIC	Draw Desc	Image
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☐ 15. Document ID: US 20010055019 A1

L6: Entry 15 of 20

File: PGPB

Dec 27, 2001

DOCUMENT-IDENTIFIER: US 20010055019 A1

TITLE: Multiple processor visibility search system and method

Detail Description Paragraph (6):

[0058] Graphics primitives (e.g. triangles) corresponding to the visible objects may be transmitted to graphics accelerator 112 for rendering and display on display device 84. Since graphics accelerator 112 operates on primitives corresponding to the visible objects, a higher percentage of rendered pixels (or supersamples) survive the z-comparison than if the graphics accelerator 112 were supplied with primitives corresponding to the full object set. In other words, the rendering hardware in graphics accelerator 112 may operate with increased efficiency.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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MMC	Draw Desc	Image
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☐ 16. Document ID: US 6496187 B1

L6: Entry 16 of 20

File: USPT

Dec 17, 2002

DOCUMENT-IDENTIFIER: US 6496187 B1

TITLE: Graphics system configured to perform parallel sample to pixel calculation

Detailed Description Text (26):

FIG. 3B presents a block diagram for one embodiment of graphics system 112 according to the present invention. Graphics system 112 may comprise a graphics processing unit (GPU) 90, one or more super-sampled sample buffers 162, and one or more sample-to-pixel calculation units 170-1 through 170-V. Graphics system 112 may also comprise one or more digital-to-analog converters (DACs) 178-1 through 178-L. Graphics processing unit 90 may comprise any combination of processor technologies. For example, graphics processing unit 90 may comprise specialized graphics processors or calculation units, multimedia processors, DSPs, or general purpose processors.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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MMC	Draw Desc	Image
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☐ 17. Document ID: US 6437796 B1

L6: Entry 17 of 20

File: USPT

Aug 20, 2002

DOCUMENT-IDENTIFIER: US 6437796 B1

TITLE: Multiple processor visibility search system and method

Detailed Description Text (6):

Graphics primitives (e.g. triangles) corresponding to the visible objects may be transmitted to graphics accelerator 112 for rendering and display on display device 84. Since graphics accelerator 112 operates on primitives corresponding to the visible objects, a higher percentage of rendered pixels (or supersamples) survive the z-comparison than if the graphics accelerator 112 were supplied with primitives corresponding to the full object set. In other words, the rendering hardware in graphics accelerator 112 may operate with increased efficiency.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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KWIC	Draw Desc	Image
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☐ 18. Document ID: US 6204859 B1

L6: Entry 18 of 20

File: USPT

Mar 20, 2001

DOCUMENT-IDENTIFIER: US 6204859 B1

TITLE: Method and apparatus for compositing colors of images with memory constraints for storing pixel data

Detailed Description Text (113):

When the new fragment is visible at one of the covered subpixel samples, then the graphics accelerator 108 invalidates the link between each covered sample and a stored fragment, if the new fragment obscures the stored fragment for that covered subpixel sample. For the indexed sparse supersampling technique, the graphics accelerator 108 maintains control bits for keeping track of the validity of each index and invalidates each index linking a covered subpixel sample to an obscured fragment. The control bits may direct the graphics accelerator 108 to use the default background color if no fragments cover a subpixel sample. For the improved A-buffer technique, the bits in the coverage mask associated with each covered subpixel sample are unchanged when the new fragment is transparent and are set to "0" when the new fragment is opaque.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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KWIC	Draw Desc	Image
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☐ 19. Document ID: US 6128000 A

L6: Entry 19 of 20

File: USPT

Oct 3, 2000

DOCUMENT-IDENTIFIER: US 6128000 A

TITLE: Full-scene antialiasing using improved supersampling techniques

Detailed Description Text (116):

When the new fragment is visible at one of the covered subpixel samples, then the graphics accelerator 108 invalidates the link between each covered sample and a stored fragment, if the new fragment obscures the stored fragment for that covered subpixel sample. For the indexed sparse supersampling technique, the graphics accelerator 108 maintains control bits for keeping track of the validity of each index and invalidates each index linking a covered subpixel sample to an obscured fragment. The control bits may direct the graphics accelerator 108 to use the default background color if no fragments cover a subpixel sample. For the improved A-buffer technique, the bits in the coverage mask associated with each covered subpixel sample are unchanged when the new fragment is transparent

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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KWIC	Draw Desc	Image
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☐ 20. Document ID: WO 200227661 A2 AU 200193158 A

L6: Entry 20 of 20

File: DWPI

Apr 4, 2002

DERWENT-ACC-NO: 2002-372173

DERWENT-WEEK: 200252

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TITLE: Implementation apparatus of full-scene anti-aliasing super-sampling to provide three-dimensional computer-generated graphics using graphics accelerator with coupled cache

Full Title Citation Front Review Classification Date Reference Sequences Attachments

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Terms	Documents
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